Sat, 27 May 2006, 9:13:24 PM EST

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#1	((nat bypass)<in>metadata)
#2	(distributed network address translation<IN>metadata)
#3	((nat bypass)<in>metadata)
#4	(distributed and network and address and translation<IN>metadata)
#5	(((distributed<in>metadata) <and> (network address translation<in>metadata))) <and> (pyr >= 1985 <and> pyr <= 2001)
#6	(((distributed<in>metadata) <and> (network and address and translation<in>metadata))) <and> (pyr >= 1985 <and> pyr <= 2001)
#7	(((distributed<in>metadata) <and> (nat<in>metadata))) <and> (pyr >= 1985 <and> pyr <= 2001)
#8	((nat<in>metadata)) <and> (pyr >= 1985 <and> pyr <= 2001)
#9	((nat<in>metadata)) <and> (pyr >= 1985 <and> pyr <= 2001)

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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	57902	nat	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2006/05/27 19:54
L2	11418248	@ad<"20010312"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2006/05/27 19:54
L3	26401	1 and 2	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2006/05/27 19:54
L4	8069	709/217-219.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2006/05/27 19:54
L5	47	3 and 4	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2006/05/27 20:00
L6	50	("6661799" "6779039" "6880089" "6895429" "6389419" "6006258" "6965930" "6381638" "6779035" "6963917" "6633560" "7051066" "6993012" "6266335" "6018619" "7050422" "7042870" "6822957" "6886103" "6963982" "6754709" "6360265" "6389462" "7003575" "7043564" "6650641" "6768743" "6725253" "6993595" "7051115" "5384777" "6985440" "6687245" "6697377" "6981278" "6993037" "6650621" "6980556" "6891830" "6353614" "7028335" "6353891" "6567405" "6781982" "6061349" "6957346" "6549516" "6606315" "6606316" "6628654").pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2006/05/27 20:01

EAST Search History

L7	50	("6687222" "6704278" "6735169" "6742045" "6836462" "6195705" "6708219" "6445704" "6886027" "7047314" "6065046" "6356863" "6266701" "6101616" "6470389" "6011782" "5600644" "6996617" "6058431" "6324582" "6909724" "6331984" "6563824" "6591306" "6829239" "7023847" "6925487" "6996621" "6667974" "6795917" "7042876" "7047561" "7020720" "5793763" "6182228" "7051116" "6118785" "5864535" "6243360" "6941366" "6584096" "6654792" "6928082" "6856624" "6327662" "6073178" "5276863" "5526483" "5799002" "6038594").pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2006/05/27 20:01
L8	100	6 7	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2006/05/27 20:01
L9	96	8 not 5	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2006/05/27 20:33
L10	50	distributed with (network adj address adj translat$5)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2006/05/27 20:34
L11	29	10 and 2	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2006/05/27 20:34

Terms used **network address translation bypass** Found **1,447** of **177,263**

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1 Architectural level synthesis: Automatic generation of operation tables for fast exploration of bypasses in embedded processors
Sanghyun Park, Eugene Earlie, Aviral Shrivastava, Alex Nicolau, Nikil Dutt, Yunheung Paek
March 2006 **Proceedings of the conference on Design, automation and test in Europe: Proceedings DATE '06**
Publisher: European Design and Automation Association
Full text available: pdf(211.83 KB) Additional Information: full citation, abstract, references

Customizing the bypasses in an embedded processor uncovers valuable trade-offs between the power, performance and the cost of the processor. Meaningful exploration of bypasses requires bypass-sensitive compiler. Operation Tables (OTs) have been proposed to perform bypass-sensitive compilation. However, due to lack of automated methods to generate OTs, OTs are currently manually specified by the designer. Manual specification of OTs is not only an extremely time consuming task, but is also highly ...

2 Hot topic: architectures and NoC (4G wireles special day): Energy efficiency vs. programmability trade-off: architectures and design principles
J. P. Robelly, H. Seidel, K. C. Chen, G. Fettweis
March 2006 **Proceedings of the conference on Design, automation and test in Europe: Proceedings DATE '06**
Publisher: European Design and Automation Association
Full text available: pdf(132.88 KB) Additional Information: full citation, abstract, references

Performance achievements on programmable architectures due to process technology are reaching their limits, since designs are becoming wire- and power-limited rather than device limited. Likewise, traditional exploitation of instruction level parallelism saturates as the conventional approach for designing wider issue machines leads to very expensive interconnections, big instruction memory footprint and high register file pressure. New architectural concepts targeted to the application domain o ...

3 Secure and security systems: Platform independent debug port controller architecture with security protection for multi-processor system-on-chip ICs
Dimitry Akselrod, Asaf Ashkenazi, Yossi Amon
March 2006 **Proceedings of the conference on Design, automation and test in Europe: Designers' forum DATE '06**
Publisher: European Design and Automation Association
Full text available: pdf(204.81 KB) Additional Information: full citation, abstract, references

A Debug Port Controller (DPC) architecture, designed for re-use in multiple System-on-Chip (SoC) Integrated Circuits (ICs) is presented. The DPC incorporates security protection against unauthorized access along with advanced debugging features such as long chain debugging, universal BIST engines control, and generic serial interfaces. An

implemented security architecture of DPC is presented together with an overall IC security scheme. DPC is the most important part of this IC security scheme. T ...

4 Media and signal processing: ASIP design and synthesis for non linear filtering in image processing

L. Fanucci, M. Cassiano, S. Saponara, D. Kammler, E. M. Witte, O. Schliebusch, G. Ascheid, R. Leupers, H. Meyr

March 2006 **Proceedings of the conference on Design, automation and test in Europe: Designers' forum DATE '06**

Publisher: European Design and Automation Association

Full text available: pdf(381.87 KB) Additional Information: full citation, abstract, references

This paper presents an Application Specific Instruction Set Processor (ASIP) design for the implementation of a class of nonlinear image processing algorithms, the Retinex-like filters. Starting from high level descriptions, first algorithmic optimization is accomplished. Then a processor architecture and an instruction set are customized with special respect to the algorithmic computations in order to achieve the specified timing at reasonable complexity. Taking advantage of the programmability ...

5 Leakage-aware circuit design: Exploiting data-dependent slack using dynamic multi-VDD to minimize energy consumption in datapath circuits

Kaushal R. Gandhi, Nihar R. Mahapatra

March 2006 **Proceedings of the conference on Design, automation and test in Europe: Proceedings DATE '06**

Publisher: European Design and Automation Association

Full text available: pdf(186.45 KB) Additional Information: full citation, abstract, references

Modern microprocessors feature wide datapaths to support large on-chip memory and to enable computation on large-magnitude operands. With device scaling and rising clock frequencies, energy consumption and power density have become critical concerns, especially in datapath circuits. Datapaths are typically designed to optimize delay for worst-case operands. However, such operands rarely occur; the most frequently occurring input operand words (comprising long strings or subwords of 0's and 1's) ...

6 Advanced SoC test scheduling: Hierarchy-aware and area-efficient test infrastructure design for core-based system chips

Anuja Sehgal, Sandeep Kumar Goel, Erik Jan Marinissen, Krishnendu Chakrabarty

March 2006 **Proceedings of the conference on Design, automation and test in Europe: Proceedings DATE '06**

Publisher: European Design and Automation Association

Full text available: pdf(210.36 KB) Additional Information: full citation, abstract, references

Multiple levels of design hierarchy are common in current-generation system-on-chip (SOC) integrated circuits. However, most prior work on test access mechanism (TAM) optimization and test scheduling is based on a flattened design hierarchy. We investigate hierarchy-aware test infrastructure design, wherein wrapper/TAM optimization and test scheduling are carried out for hierarchical SOCs for two practical design scenarios. In the first scenario, the wrapper and TAM implementation for the embedd ...

7 Application examples with leading edge design methodology: SAVS: a self-adaptive variable supply-voltage technique for process- tolerant and power-efficient multi-issue superscalar processor design

Hai Li, Yiran Chen, Kaushik Roy, Cheng-Kok Koh

January 2006 **Proceedings of the 2006 conference on Asia South Pacific design automation ASP-DAC '06**

Publisher: ACM Press

Full text available: pdf(390.55 KB) Additional Information: full citation, abstract, references

Technology scaling and sub-wavelength optical lithography is associated with significant process variations. We propose a self-adaptive variable supply-voltage scaling (SAVS)

technique for multi-issue out-of-order pipeline to improve parametric yield with minimal power dissipation. Our error-correction circuitry and recovery mechanism allow the proposed fault-tolerant pipeline to work at a dynamically tuned supply voltage with a very low error rate. Experiments on an 8-issue, out-of-order supers ...

8 "Flea-flicker" Multipass Pipelining: An Alternative to the High-Power Out-of-Order Offense

Ronald D. Barnes, Shane Ryoo, Wen-mei W. Hwu

November 2005 **Proceedings of the 38th annual IEEE/ACM International Symposium on Microarchitecture MICRO 38**

Publisher: IEEE Computer Society

Full text available: pdf(346.82 KB) Publisher Site Additional Information: full citation, abstract

As microprocessor designs become increasingly powerand complexity-conscious, future microarchitectures must decrease their reliance on expensive dynamic scheduling structures. While compilers have generally proven adept at planning useful static instruction-level parallelism, relying solely on the compiler¿s instruction execution arrangement performs poorly when cache misses occur, because variable latency is not well tolerated. This paper proposes a new microarchitectural model, multipass pipel ...

9 Privacy and anonymity: Tracking anonymous peer-to-peer VoIP calls on the internet

Xinyuan Wang, Shiping Chen, Sushil Jajodia

November 2005 **Proceedings of the 12th ACM conference on Computer and communications security CCS '05**

Publisher: ACM Press

Full text available: pdf(248.17 KB) Additional Information: full citation, abstract, references, index terms

Peer-to-peer VoIP calls are becoming increasingly popular due to their advantages in cost and convenience. When these calls are encrypted from end to end and anonymized by low latency anonymizing network, they are considered by many people to be both secure and anonymous.In this paper, we present a watermark technique that could be used for effectively identifying and correlating encrypted, peer-to-peer VoIP calls even if they are anonymized by low latency anonymizing networks. This result is in ...

Keywords: VoIP, VoIP tracing, anonymous VoIP calls, anonymous communication, peer-to-peer

10 IP lookup and packet classification: Network processor acceleration for a Linux* netfilter firewall

Kristen Accardi, Tony Bock, Frank Hady, Jon Krueger

October 2005 **Proceedings of the 2005 symposium on Architecture for networking and communications systems ANCS '05**

Publisher: ACM Press

Full text available: pdf(485.59 KB) Additional Information: full citation, abstract, references, index terms

Network firewalls occupy a central role in computer security, protecting data, compute, and networking resources while still allowing useful packets to flow. Increases in both the work per network packet and packet rate make it increasingly difficult for general-purpose processor based firewalls to maintain line rate. In a bid to address these evolving requirements we have prototyped a hybrid firewall, using a simple firewall running on a network processor to accelerate a Linux* Netfilter Firewa ...

Keywords: hybrid firewall, netfilter, network firewall, network processor, prototype, throughput

11 Challenge papers: Challenge: CeTV and Ca-Fi - cellular and Wi-Fi over CATV

Erez Biton, Danny Sade, Dan Shklarsky, Mota Zussman, Gil Zussman

August 2005 **Proceedings of the 11th annual international conference on Mobile computing and networking MobiCom '05**
Publisher: ACM Press
Full text available: pdf(493.06 KB) Additional Information: full citation, abstract, references, index terms

This paper introduces a novel concept that enables transmitting wireless communication over CATV networks. We present the architecture of a system for Cellular Communication over CATV (CeTV) and review the required modifications to the cable network. These modifications affect only the cable network, thereby enabling the system to operate with unmodified cellular phones. In addition to improving in-building coverage, the CeTV system significantly increases the capacity of the cellular network. W ...

Keywords: CATV, IEEE 802.11, MAC, cellular networks, polling, wireless LANs

12 Low power memory: Snug set-associative caches: reducing leakage power while improving performance
Jia-Jhe Li, Yuan-Shin Hwang
August 2005 **Proceedings of the 2005 international symposium on Low power electronics and design ISLPED '05**
Publisher: ACM Press
Full text available: pdf(154.66 KB) Additional Information: full citation, abstract, references, index terms

As transistors keep shrinking and on-chip data caches keep growing, static power dissipation due to leakage of caches takes an increasing fraction of total power in processors. Several techniques have already been proposed to reduce leakage power by turning off unused cache lines. However, they all have to pay the price of performance degradation. This paper presents a cache architecture, the *Snug Set-Associative* (*SSA*) cache, that does not only cut most of static power dissipation ...

Keywords: leakage power, set-associative caches

13 Session 2: value: An asymmetric clustered processor based on value content
R. González, A. Cristal, M. Pericas, M. Valero, A. Veidenbaum
June 2005 **Proceedings of the 19th annual international conference on Supercomputing ICS '05**
Publisher: ACM Press
Full text available: pdf(1.60 MB) Additional Information: full citation, abstract, references, index terms

This paper proposes a new organization for clustered processors. Such processors have many advantages, including improved implementability and scalability, reduced power, and, potentially, faster clock speed. Difficulties lie in assigning instructions to clusters (steering) so as to minimize the effect of inter-cluster communication latency. The *asymmetric* clustered architecture proposed in this paper aims to increase the IPC and reduce power consumption by using two different types of in ...

Keywords: cluster architectures, content aware architectures

14 A sample-based cache mapping scheme
Rong Xu, Zhiyuan Li
June 2005 **ACM SIGPLAN Notices , Proceedings of the 2005 ACM SIGPLAN/SIGBED conference on Languages, compilers, and tools for embedded systems LCTES'05**, Volume 40 Issue 7
Publisher: ACM Press
Full text available: pdf(164.54 KB) Additional Information: full citation, abstract, references, index terms

Applications running on the StrongARM SA-1110 or XScale processor cores can specify cache mapping for each virtual page to achieve better cache utilization. In this work, we describe a method to efficiently perform cache mapping. Under this scheme, we select a

number of loops for sampling. These loops are selected automatically based on clock profiling information. We formulate the optimal cache mapping problem as an Integer Linear Programming (ILP) problem. Experiments performed on 14 test prog ...

Keywords: cache bypass, cache mapping, handheld devices, mini cache, profiling, trace sampling

15 Static strands: safely collapsing dependence chains for increasing embedded power efficiency

Peter G. Sassone, D. Scott Wills, Gabriel H. Loh

June 2005 **ACM SIGPLAN Notices , Proceedings of the 2005 ACM SIGPLAN/SIGBED conference on Languages, compilers, and tools for embedded systems LCTES'05**, Volume 40 Issue 7

Publisher: ACM Press

Full text available: pdf(274.43 KB) Additional Information: full citation, abstract, references, index terms

Modern embedded processors are designed to maximize execution efficiency--the amount of performance achieved per unit of energy dissipated while meeting minimum performance levels. To increase this efficiency we propose utilizing *static strands*, dependence chains without fan-out which are exposed by a compiler pass. These dependent instructions are resequenced to be sequential and annotated to communicate their location to the hardware. Importantly, this modified application is binary com ...

Keywords: architecture, dependency collapsing, embedded, energy, sequentiality

16 Architectural support for communication: Cache coherence support for non-shared bus architecture on heterogeneous MPSoCs

Taeweon Suh, Daehyun Kim, Hsien--Hsin S. Lee

June 2005 **Proceedings of the 42nd annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(652.43 KB) Additional Information: full citation, abstract, references, index terms

We propose two novel integration techniques □ *bypass* and *bookkeeping*□in the memory controller to address the cache coherence compatibility issue of a non-shared bus heterogeneous MPSoC. The bypass approach is an inexpensive and efficient solution for computation-bound applications while the bookkeeping approach eliminating unnecessary forwarding traffic offers an alternative for bandwidth-limited applications. Our RTOS kernel simulations show up to 6.65x speedup over the ...

Keywords: MPSoC, cache coherence, heterogeneous, inter-processor communication, real-time and embedded systems

17 Path slicing

Ranjit Jhala, Rupak Majumdar

June 2005 **ACM SIGPLAN Notices , Proceedings of the 2005 ACM SIGPLAN conference on Programming language design and implementation PLDI '05**, Volume 40 Issue 6

Publisher: ACM Press

Full text available: pdf(303.79 KB) Additional Information: full citation, abstract, references, index terms

We present a new technique, *path slicing*, that takes as input a possibly infeasible path to a target location, and eliminates all the operations that are irrelevant towards the reachability of the target location. A path slice is a subsequence of the original path whose infeasibility guarantees the infeasibility of the original path, and whose feasibility guarantees the existence of some feasible variant of the given path that reaches the target location even though the given path may its ...

Keywords: counterexample analysis, program slicing

18 Hardware synthesis from guarded atomic actions with performance specifications
D. L. Rosenband
May 2005 **Proceedings of the 2005 IEEE/ACM International conference on Computer-aided design ICCAD '05**
Publisher: IEEE Computer Society
Full text available: pdf(267.38 KB) Additional Information: full citation, abstract

We present a new hardware synthesis methodology for guarded atomic actions (or rules), which satisfies performance-related scheduling specifications provided by the designer. The methodology is based on rule composition, and relies on the fact that a rule derived by the composition of two rules behaves as if the two rules were scheduled simultaneously. Rule composition is a well understood transformation in the TRS theoretical framework; however, previous rule composition approaches resulted in ...

19 Continuous Optimization
May 2005 **ACM SIGARCH Computer Architecture News , Proceedings of the 32nd Annual International Symposium on Computer Architecture ISCA '05**, Volume 33 Issue 2
Publisher: IEEE Computer Society, ACM Press
Full text available: pdf(233.53 KB) Additional Information: full citation, abstract, index terms

This paper presents a hardware-based dynamic optimizer that continuously optimizes an applicationýs instruction stream. In continuous optimization, dataflow optimizations are performed using simple, table-based hardware placed in the rename stage of the processor pipeline. The continuous optimizer reduces dataflow height by performing constant propagation, reassociation, redundant load elimination, store forwarding, and silent store removal. To enhance the impact of the optimizations, the optimi ...

20 RENO: A Rename-Based Instruction Optimizer
May 2005 **ACM SIGARCH Computer Architecture News , Proceedings of the 32nd Annual International Symposium on Computer Architecture ISCA '05**, Volume 33 Issue 2
Publisher: IEEE Computer Society, ACM Press
Full text available: pdf(256.23 KB) Additional Information: full citation, abstract, index terms

RENO is a modified MIPS R10000 register renamer that uses map-table "short-circuiting" to implement dynamic versions of several well-known static optimizations: move elimination, common subexpression elimination, register allocation, and constant folding. Because it implements these optimizations dynamically, RENO can apply optimizations in certain situations where static compilers cannot. Several of RENOýs component optimizations have been previously proposed as independent mechanisms. Unified ...

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